

# METHOD FOR PROGRAMMING NON-VOLATILE MEMORY

## DESCRIPTION

### BACKGROUND OF THE INVENTION

**[Para 1]** Field of the Invention

**[Para 2]** The present invention relates to a method for operating a memory device, and more particularly, to a method for programming a non-volatile memory.

**[Para 3]** Description of Related Art

**[Para 4]** Since programmable non-volatile memory can be used to improve flexibility of circuit design and has reduced weight and capability to retain data even when the power is down, it is widely applied in related fields. In conventional methods for programming programmable non-volatile memory, fixed reference levels are always used to distinguish the data storage states (referred to as "storage state" hereinafter) of the memory cells, and the reference level may be a reference level of current or threshold voltage  $V_T$ .

**[Para 5]** For example, a one-time programmable (OTP) memory capable of storing one bit per cell is programmed using one fixed reference level, while a multi-level cell (MLC) memory or a multi-time programmable (MTP) memory is programmed using multiple fixed reference levels, as shown in FIGs. 1-2. Briefly, FIG. 1(A) shows an ideal relationship between multiple fixed reference levels and the cell level distributions of all storage states in a MLC memory of two bits per cell. FIG. 2(A) shows ideal relationships between multiple fixed reference levels and the cell level distributions of both storage states in a MTP

memory after the MTP memory is programmed first time and second time, respectively.

[Para 6] However, using fixed reference levels tends to restrict the programming speed of a MLC or MTP non-volatile memory. This is because the degree of pumping charges into a memory cell is difficult to stably control when the programming speed is increased, so that over-programming easily occurs to broaden the level distribution of memory cells. Therefore, as shown in FIG. 1(B) or 2(B), the inter-state window (represented by “w”) between two storage states of the MLC or MTP memory becomes narrower, so that reading errors are easily caused.

## SUMMARY OF THE INVENTION

[Para 7] Accordingly, one object of this invention is to provide a method for programming a non-volatile memory, which can avoid the problems of over-programming and the inter-state window narrowing.

[Para 8] Another object of this invention is to provide a method for programming a non-volatile memory, which allows a higher programming speed to be used.

[Para 9] Yet another object of this invention is to provide a method for programming a multi-level cell (MLC) non-volatile memory, which is based on the method for programming a non-volatile memory of this invention.

[Para 10] Still another object of this invention is to provide a method for programming a multi-time programmable (MTP) non-volatile memory, which is based on the method for programming a non-volatile memory of this invention.

[Para 11] In the method for programming a non-volatile memory of this invention, a reference level is selected according to the level distribution of the memory cells in a storage state, and then predetermined memory cells are programmed to the next storage state according to the reference level. The

reference level falls between the cell level distribution of the storage state and that of the next storage state. Here, the so-called "level" may be a current level or a threshold voltage level depending on the type of the non-volatile memory.

[Para 12] In a preferred embodiment of this invention, the cell level of the next storage state is higher than that of the current storage state, and the reference level falls between the highest cell level of the current storage state and the lowest cell level of the next storage state. In addition, the non-volatile memory may be a one-time programmable (OPT) memory, a multi-time programmable (MTP) memory, a multi-level cell (MLC) memory, or a programmable resistor with erase-less memory (PREM), etc.

[Para 13] The method for programming a MLC non-volatile memory of this invention starts from the programming of the storage state with lowest level, wherein the MLC non-volatile memory can have a first storage state up to an  $N^{\text{th}}$  storage state in an ascending order. Firstly, the initial value of the storage state indicator  $i$  is set to 1. The following steps are then repeated until the  $N^{\text{th}}$  storage state has been programmed: (a) an  $i^{\text{th}}$  reference level is selected according to the level distribution of the memory cells in the  $i^{\text{th}}$  storage state; and (b) predetermined memory cells are programmed to an  $(i+1)^{\text{th}}$  storage state according to the  $i^{\text{th}}$  reference level. The value of  $i$  is incremented by 1 before each repetition, and the  $i^{\text{th}}$  reference level falls between the highest cell level of the  $i^{\text{th}}$  storage state and the lowest cell level of the  $(i+1)^{\text{th}}$  storage state.

[Para 14] The method for programming a MTP non-volatile memory of this invention is described as follows. In this method, first, a reference level is selected according to the level distribution of all memory cells. Then, each memory cell is reset to a first storage state, and a part of the memory cells are programmed to a second storage state according to the reference level. The reference level falls between the highest cell level of the first storage state and the lowest cell level of the second storage state.

[Para 15] Since the method for programming a non-volatile memory of this invention actively selects a reference level according to the cell level

distribution of each storage state and then programs predetermined memory cells to the next storage state according to the reference level, the inter-state window is not narrowed. Therefore, this invention can reduce the reading errors. In addition, since the reference level is adjustable to match the real level distribution of memory cells, the method of this invention allows a broader level distribution of memory cells. That is, a higher programming speed is allowed.

[Para 16] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[Para 17] FIG. 1(A) schematically shows an ideal relationship between the fixed reference levels and the level distributions of the memory cells in a MLC memory of two bits per cell, and FIG. 1(B) schematically shows an example of over-programming.

[Para 18] FIG. 2(A) schematically shows an ideal relationship between the fixed reference levels and the cell level distributions of both storage states in a MTP memory after the MTP memory is programmed first time and second time, respectively, and FIG. 2(B) schematically shows an example of over-programming.

[Para 19] FIG. 3 is a flow chart illustrating a method for programming a MLC non-volatile memory according to a preferred embodiment of this invention.

[Para 20] FIG. 4 is a flow chart illustrating a method for programming a MTP non-volatile memory according to the preferred embodiment of this invention.

[Para 21] FIG. 5 schematically shows an example of the method for programming a MLC non-volatile memory of two bits per cell according to the preferred embodiment of this invention.

[Para 22] FIG. 6 schematically shows an example of the method for programming a MTP non-volatile memory according to the preferred embodiment of this invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Para 23] It is noted that though the methods for programming a MLC non-volatile memory and a MTP non-volatile memory, respectively, are exemplified hereinafter, this invention can also be applied to a less complicated OTP memory or a more complicated MLC or MTP non-volatile memory according to the spirit of this invention.

[Para 24] FIG. 3 is a flow chart illustrating a method for programming a MLC non-volatile memory according to the preferred embodiment of the present invention. When the programming is just started (step 310), the initial value of the storage state indicator "i" is set to 1. Then, an  $i^{\text{th}}$  reference level is selected according to the level distribution of the memory cells in the  $i^{\text{th}}$  storage state (step 320), and its value is higher than the highest cell level of the  $i^{\text{th}}$  storage state. Then, predetermined memory cells are programmed to an  $(i+1)^{\text{th}}$  storage state according to the  $i^{\text{th}}$  reference level (step 330), and the lowest cell level of the  $(i+1)^{\text{th}}$  storage state is higher than the  $i^{\text{th}}$  reference level. Then, it is determined whether the programming is completed or not (step 340), i.e., whether the storage state of highest level has been programmed or not. If the programming is not yet completed, the process returns to step 320 and repeats the steps 320 to 340 until the programming of the storage state of highest level is completed (step 350), wherein the value of i is incremented by 1 before each repetition.

[Para 25] FIG. 4 is a flow chart illustrating a method for programming a MTP non-volatile memory according to the preferred embodiment of the present invention. After the programming is started (step 410), a reference level is selected according to the level distribution of the memory cells in the MTP non-volatile memory (step 420), having a value higher than the highest level of

the memory cells. Meanwhile, the storage state of each memory cell is reset to a specific storage state (step 420). Then, a predetermined part of the memory cells are programmed to another storage state according to the reference level (step 430), thus completing the programming operation (step 440). The lowest cell level of the latter storage state is higher than the reference level.

[Para 26] FIG. 5 schematically shows an example of the method for programming a MLC non-volatile memory according to the preferred embodiment of this invention, wherein each memory cell can store 2 bits and has four storage states, 00, 01, 10, and 11, in an ascending order of cell level. As shown in FIG. 5, the level distribution of all memory cells that have not been programmed is determined firstly, which is referred as the cell level distribution of the first storage state (00), and then a level higher than the highest cell level of the storage state 00 is selected as a first reference level. Thereafter, predetermined memory cells are programmed to the second storage state (01) according to the first reference level, and the lowest cell level of the storage state 01 is higher than the first reference level. Then, similar steps are repeated to determine a second reference level, program the third storage state (10), determine the third reference level and program the fourth storage state (11) sequentially.

[Para 27] In addition, each reference level mentioned above can be selected from multiple candidate reference levels which are predetermined before the programming. Referring to FIG. 5, for example, multiple candidate reference levels A-K are predetermined before the programming. After the cell level distribution of the storage state "00" is determined, the candidate reference level A satisfying a predetermined inter-state window is selected from the candidate reference levels A-K whose values are higher than the highest cell level of the storage state "00" as a first reference level. After the programming of the storage state "01" according to the first reference level is completed, the candidate reference level D satisfying a predetermined inter-state window is selected from the candidate reference levels D-K whose levels are higher than the highest cell level of the storage state "01" as a second reference level. Similarly, after the programming of the storage state "10" according to the

second reference level is completed, the candidate reference level G satisfying a predetermined inter-state window is selected from the candidate reference levels G-K whose levels are higher than the highest cell level of the storage state "10" as a third reference level. Finally, the storage state "11" is programmed according to the third reference level.

[Para 28] Furthermore, the MLC non-volatile memory mentioned above is, for example, a programmable resistor with erase-less memory (PREM), in which each memory cell includes a P-type semiconductor layer and a N-type semiconductor layer which are isolated by a very thin dielectric layer. To program a memory cell, the current level of the same is set by applying a voltage thereto to cause accumulated breakdown effect of the dielectric layer, wherein the reference level is a current level. A PREM is characterized in that the cell current increases along with increases of the programming voltage and the programming time, so that a memory cell can be programmed to one of multiple different levels. Therefore, the PREM can be used as a MLC non-volatile memory. Meanwhile, since the accumulated breakdown effect is an irreversible process, the programming must start from the storage state of lowest level when a PREM is used as the MLC non-volatile memory.

[Para 29] In addition, although the case of each memory cell storing 2 bits is exemplified above, the scope of this invention is not necessarily restricted to it. This invention can also be applied to a programmable non-volatile memory that stores 3 or more bits per cell.

[Para 30] FIG. 6 schematically shows an example of the method for programming a MTP non-volatile memory according to the preferred embodiment of this invention, wherein each memory cell stores one bit and the cell level of the storage state "1" is higher than that of the storage state "0". As shown in FIG. 6, in the first-time programming, the level distribution of all memory cells having not been programmed is determined, and then a first reference level is selected according to the level distribution, having a value higher than the highest level of the memory cells. Then, the storage state of each memory cell is reset to the state "0", and predetermined memory cells are programmed to the storage state "1" according to the first reference

level, wherein the lowest level of the programmed memory cells is higher than the reference level. Afterwards, when a second-time programming is required, the cell level distribution of the storage state "1" is determined, and a second reference level is selected according to the cell level distribution, having a value higher than the highest cell level of the storage state "1". Then, the storage state of each memory cell is reset to the state "0", and predetermined memory cells are programmed to the storage state "1" according to the second reference level, wherein the lowest level of the newly programmed memory cells is higher than the second reference level. With similar steps, the third-time programming and subsequent programming processes can be performed.

[Para 31] Similarly, each reference level mentioned above can be selected from multiple candidate reference levels which are predetermined before the first-time programming. Referring to FIG. 6, in such a case, multiple candidate reference levels A-K are predetermined before the programming. After the level distribution of all memory cells having not been programmed is determined, the candidate reference level A satisfying the required inter-state window is selected from the candidate reference levels A-K whose levels are higher than the highest level of the memory cells as a reference level. In the subsequent second-time programming, after the cell level distribution of the storage state "1" is determined, the candidate reference level D satisfying the required inter-state window is selected from the candidate reference levels D-K whose levels are higher than the highest cell level of the storage state "1" as a reference level.

[Para 32] In addition, the MTP non-volatile memory mentioned above is, for example, a PREM described above. As mentioned before, since the memory cell current of a PREM increases along with increase of the programming time, it is possible to raise the current level of a memory cell more than one times within a valid range, as shown in FIG. 6. Therefore, a PREM can be used as a MTP non-volatile memory mentioned above. In addition, since the accumulated breakdown effect is an irreversible process, it is only possible to raise the current level of a memory cell in the programming of each time.

**[Para 33]** Since the method for programming a non-volatile memory of this invention selects a reference level according to the real cell level distribution of a storage state, the inter-state window is not narrowed to cause reading errors. In addition, since the reference level is adjustable to satisfy the real cell level distribution of the storage state, the method of this invention allows a broader level distribution of a storage state. In other words, a higher programming speed is allowed.

**[Para 34]** It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.